In the Claims

Claims 1-29 (Canceled)

Claim 30. (Previously Presented): A method of forming memory cells in an array including:

forming a first memory cell including a first access transistor and a first data storage element, a first load electrode of the first access transistor being coupled to the first data storage element via a first storage node formed on a substrate;

forming a second memory cell including a second access transistor and a second data storage element, a first load electrode of the second access transistor being coupled to the second data storage element via a second storage node formed on the substrate, wherein forming the first and second memory cells includes forming the first and second access transistors to have a first threshold voltage; and

forming an isolation gate between the first and second storage nodes and configured to provide electrical isolation therebetween, wherein forming the isolation gate includes forming the isolation gate to have a second threshold voltage greater than the first threshold voltage.

Claim 31. (Previously Presented): The method of claim 30, wherein forming first and second access transistors includes forming first gate dielectrics with a first thickness for each of the first and second access transistors, and wherein forming the isolation gate includes forming a second gate dielectric comprising an isolation gate dielectric to have a second thickness that is greater than the first thickness.

Claim 32. (Previously Presented): The method of claim 30, wherein forming first and second access transistors includes forming first gate dielectrics with a first thickness for each of the first and second access transistors and further comprising forming an isolation gate dielectric by:

forming a shallow trench;

forming an isolation gate dielectric by a deposition process that fills the shallow trench with a dielectric material; and

planarizing the dielectric material using chemical-mechanical polishing, wherein the isolation gate dielectric is formed to have a second thickness that is greater than the first thickness.

Claim 33. (Previously Presented): The method of claim 32, further comprising implanting dopant into the shallow trench prior to forming the isolation gate dielectric.

Claim 34. (Previously Presented): The method of claim 30, wherein forming first and second access transistors includes forming first gate dielectrics with a first thickness for each of the first and second access transistors and further comprising forming an isolation gate dielectric to have a second thickness that is between thirty percent and seventy percent thicker than the first thickness.

Claim 35. (Previously Presented): The method of claim 30, wherein forming first and second access transistors includes forming first gate dielectrics with a first thickness of about fifty Angstroms for each of the first and second access transistors and further comprising forming an isolation gate dielectric to have a second thickness in a range of from about seventy Angstroms to about one hundred Angstroms.

Claim 36. (Previously Presented): The method of claim 31, wherein forming the first and second memory cells includes forming the first and second gate dielectrics to be silicon dioxide.

Claim 37. (Previously Presented): The method of claim 30, wherein forming memory cells comprises forming DRAM memory cells and wherein forming first and second memory cells includes forming first and second memory cells wherein the first and second data storage elements comprise capacitors.

Claim 38. (Previously Presented): The method of claim 30, wherein forming the first and second memory cells includes forming DRAM memory cells, and further comprising:

forming each of the access transistors to include a second load electrode coupled to a respective bitline contact; and

implanting a halo implant in each of the access transistors only on a bitline contact side thereof to provide the first threshold voltage determined in part by the halo implant.

Claim 39. (Previously Presented): The method of claim 30, wherein the first and second data storage elements comprise capacitors.